REMARKS

In the Office Action mailed August 28, 2002, the Examiner stated that the oath or declaration is defective. Applicants are filing a new oath or declaration by a supplemental response in compliance with 37 C.F.R. § 1.67(a).

In the Office Action, the Examiner objected to the drawings as failing to comply with 37 C.F.R. § 1.84(p)(5). Applicants have added reference numeral 400 referring to "substrate" and reference numeral 402 referring to "intermediate layer" to the paragraph beginning on line 12 on page 21. Applicants respectfully request that the Examiner withdraw the objection to the drawings.

In the Office Action, the Examiner rejected Claims 17, 18, and 21 under 35 U.S.C. § 102(b) as being anticipated by Bacchetta et al. (U.S. Patent No. 5,627,403) ("Bacchetta"). To the extent that the rejection applies to the amended claims, Applicants respectfully traverse the rejection.

Applicants' amended Claim 17 and dependent Claims 18 and 21 recite the limitations of, "an oxide layer, an adhesion layer formed over said oxide layer, and a first passivation formed on said adhesion layer." Applicants respectfully submit that Bacchetta does not teach or suggest the desirability of the structure as recited in Applicants' amended Claim 17 and dependent Claims 18 and 21.

Applicants respectfully submit that Bacchetta teaches dielectric (1) of silicon nitride or silicon oxynitride, with oxide layer (2) of silicon dioxide, then dielectric (3) of silicon nitride or silicon oxynitride. "In accordance with the invention, a thin layer of an oxide (silicon dioxide in the preferred embodiment) is formed at the interface between a first layer of a dielectric material and a successive layer of dielectric material, specifically silicon oxynitride and/or silicon nitride. This intermediate oxide acts as an adhesion layer between the two superimposed layers." (Bacchetta, col. 3, lines 42-49.)

Applicants respectfully submit that Bacchetta's oxide layer (2) laminate (shown in Figures 1 and 2 of Bacchetta) does not have the structure of an adhesion layer formed over an oxide layer, and a first passivation layer formed on the adhesion layer. In

Bacchetta, the oxide layer acts as the adhesive, while in Applicants' invention, an adhesion layer is formed to act in one regard as an adhesive between the oxide layer and the first passivation layer. Bacchetta does not teach or suggest the desirability of an adhesion layer acting as an adhesive between an oxide layer and a first passivation layer.

Applicants respectfully request that the Examiner withdraw the rejection to Claims 17, 18, and 21 under 35 U.S.C. § 102(b) as being anticipated by Bacchetta.

In the Office Action, the Examiner rejected Claim 23 under 35 U.S.C. § 102(b) as being anticipated by Takiar et al. (U.S. Patent No. 4,723,197) ("Takiar"). To the extent that the rejection applies to the amended claim, Applicants respectfully traverse the rejection.

Applicants respectfully submit that amended Claim 23 recites the limitations of a silicon dioxide insulating layer, a silicon oxynitride adhesion layer formed on said silicon dioxide insulating layer, and a silicon nitride hard passivation layer formed on said silicon oxynitride adhesion layer. Claim 23 recites a laminate structure of an adhesion layer of silicon oxynitride which acts as an adhesive between a silicon dioxide insulating layer and a silicon nitride hard passivation layer.

Applicants respectfully submit that Takiar does not teach or suggest the desirability of the limitations of Applicants' Claim 23. Specifically, Takiar recites a silicon dioxide passivation layer (16), which is adjacent to substrate (10) and silicon nitride passivation layer (18). Silicon oxynitride layer (22) is two layers away from silicon dioxide passivation layer (16) (see Takiar Figures 2 and 3). Applicants respectfully submit that Takiar does not teach or suggest the desirability of a silicon oxynitride adhesion layer formed on a silicon dioxide insulating layer.

Applicants respectfully request that the Examiner withdraw the rejection to Claim 23 under 35 U.S.C. § 102(b) as being anticipated by Takiar.

In the Office Action, the Examiner rejected Claims 19, 20, and 22 under 35 U.S.C. § 103(a) as being obvious over Bacchetta in view of Mu et al. (U.S. Patent No. 5,612,254)

("Mu"). To the extent that the rejection applies to the amended claims, Applicants respectfully traverse the rejection.

In regards to Claim 19, the Examiner stated that Bacchetta fails to disclose the insulating layer including silicon dioxide. Applicants respectfully submit that Mu does not remedy the defects of Bacchetta regarding Claim 17 (from which Claim 19 depends) discussed above.

In addition, Bacchetta teaches an oxide layer (2), as an adhesive but does not teach an oxide layer as the protective dielectric (1). Bacchetta teaches, "The layer 2 provides an adhesive layer between the layers 1 and 3, and serves no specific passivation function." (Bacchetta, col. 4, lines 9-10). Applicants respectfully submit that there is no motivation or suggestion to combine a silicon dioxide layer as found in Mu with the protective dielectric (1) of Bacchetta, since Bacchetta teaches an oxide layer (2) as an adhesive between the two protective dielectric layers (1 and 3) and teaches against the oxide layer as a passivation layer. Applicants respectfully request that the Examiner withdraw the rejections to Claim 19 under 35 U.S.C. § 103(a).

In regards to Claim 20, the Examiner stated that Bacchetta fails to disclose that the adhesion layer includes silicon oxynitride. Applicants respectfully submit that Mu fails to remedy the defects of Bacchetta discussed above regarding Claim 17 (from which Claim 20 depends). In addition, Bacchetta teaches against an adhesion layer of silicon oxynitride, since Bacchetta teaches an oxide layer (2) which is used to increase the adhesion between two protective dielectric layers (1 and 3) which are made of silicon nitride or silicon oxynitride. It would not have been obvious to increase the adhesion between silicon oxynitride layers by replacing the oxide layer with silicon oxynitride. Bacchetta teaches using an oxide as the adhesive, not silicon oxynitride, "The adhesive properties of the oxide layer, which is interposed between two dielectric layers in accordance with this invention, have been verified experimentally. . . . Experimental tests point to the likelihood that a thin layer of an oxide other than of silicon, e.g., of titanium, may also be used." (Bacchetta, col. 4, lines 53-55 and 65-67.) Applicants respectfully request that the Examiner withdraw the rejection to Claim 20 under 35 U.S.C. § 103(a).

In regards to Claim 22, the Examiner stated that Bacchetta fails to disclose that the second passivation layer includes polyamide. Applicants respectfully submit that Mu does not remedy the defects of Bacchetta discussed above regarding Claims 17 and 18 (from which Claim 22 depends). Specifically, Mu and Bacchetta, alone or in combination, do not teach or suggest the desirability of an adhesion layer between an oxide layer and a first passivation layer, as recited in Applicants' independent Claim 17 and dependent Claim 22 which depends therefrom. Applicants respectfully request that the Examiner withdraw the rejection to Claim 22 for at least the reasons stated above.

In the Office Action, the Examiner rejected Claim 24 under 35 U.S.C. § 103(a) as being obvious over Takiar in view of Bryant et al. (U.S. Patent No. 5,698,456) ("Bryant"). To the extent that the rejection applies to the amended claim, Applicants respectfully traverse the rejection.

Applicants respectfully submit that Bryant does not remedy the defect of Takiar discussed above regarding Claim 23 (from which Claim 24 depends). Specifically, Takiar and Bryant, alone or in combination, do not teach or suggest the desirability of a silicon oxynitride adhesion layer between a silicon dioxide insulating layer and a silicon nitride hard passivation layer as recited in Applicants' independent Claim 23 and dependent Claim 24.

Applicants respectfully request that the Examiner withdraw the rejection to Claim 24 under 35 U.S.C. § 103(a) for at least the reasons cited above.

Attached hereto is a marked-up version of the changes made to the abstract and claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

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CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance, and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 11/27/02

William E. Hickman, Reg. No. 46,771

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING:
I hereby certify that this correspondence is being deposited as First Class Mail with the United States Postal Service in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on November 27, 2002.

Nadya Gordon 11/27/02
Nadya Gordon *Date*

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION

On page 15, starting on line 19, the paragraph was amended as follows:

Figure 11 illustrates a cross-sectional side view through the portions of the integrated circuits in connection with a further processing step of the embodiment of the process described herein. Hard passivation layer 155 is deposited over a top surface of adhesion layer 150, bond pads 110 and 115, guard rings 120 and 125, and E-Test pad 130. Hard passivation layer 155 serves to protect the integrated circuit from environmental contaminants, particularly from moisture and ions. Deposition of hard passivation layer 155 may be by conventional deposition processes, such as plasma enhanced chemical vapor deposition (PECVD). Hard passivation layer 155 may include, for example, silicon nitride, boron nitride, or carbon nitride. In one embodiment of the process according to the present invention, hard passivation layer 155 includes silicon nitride. Silicon nitride hard passivation layer 155 contains nitrogen (N), the same chemical element found in nitrous oxide gas 145. Hard passivation layer 155 is conformally deposited over the above-mentioned structures to a thickness of about 1μm or less. Soft passivation layer 160 is then deposited on hard passivation layer 155. Soft passivation layer 160 may also be deposited by PECVD. In one embodiment of the process according to the present invention, soft passivation layer 160 is a photodefinable polyimide layer spun to a thickness of approximately 11.5 μm, which reduces to a thickness of approximately 3 μm at the end of processing.

On page 17, starting on line 12, the paragraph was amended as follows:

Once soft passivation layer 160 is cured, the exposed hard passivation layer 155 is etched to form openings to bond pads 110 and 115 and to remove hard passivation layer material from scribe street area 140. Adhesion layer 150 is also removed in these areas. In the embodiment where hard passivation layer 155 includes silicon nitride and adhesion layer 150 includes silicon oxynitride, a plasma etch process that removes both silicon oxynitride and silicon nitride is performed. In the case where the integrated

circuits include a multi-layer conductive material such as the TiN ARC layer described above, this material may be removed at this step. A typical etchant that may etch silicon oxynitride, silicon nitride, and the TiN ARC layer may include for example, a NF_3/He and SF_6/He.

On page 19, starting on line 18, the paragraph was amended as follows:

Figures 16-18 illustrate cross-sectional views through the portions of the integrated circuits in connection with the process described in connection with **Figures 9-15** for use with a C4 platform integrated circuit devices 200 and 205. In **Figure 16**, integrated circuit devices 200 and 205 are separated by a scribe street area 240. Integrated circuit devices 200 and 205 include conductive material bond pads 210 and 215, respectively, and guard rings 220 and 225, respectively. Scribe street area 240 contains E-Test pad 230. Adjacent the top surface of oxide layer 28 is an adhesion layer 250 of silicon oxynitride, for example. Overlying the conductive structures of the wafer is ~~a first~~ hard passivation layer 255 of silicon nitride, for example. In one embodiment, the silicon oxynitride layer is formed by exposing oxide layer 28 of silicon dioxide to a nitrous oxide (N_2O) treatment. Overlying hard passivation layer 255 is soft passivation layer 260 of photodefinable polyimide, for example. For a more detailed description of the formation of hard passivation layer 255, soft passivation layer 260, and adhesion layer 250, reference is made to **Figures 9-12** and the accompanying text.

On page 21, starting on line 12, the paragraph was amended as follows:

Figure 20 illustrates a portion of a semiconductor device with spacers formed thereon. Spacers 408 are formed along the sidewalls of a hardmask 406 and a gate 404 of a Complementary Metal Oxide Semiconductor (CMOS), for example. Spacers 408 are passivated in an oxide layer 410, an adhesion layer 412, and a passivation layer 414 in accordance with an embodiment of the present invention. Spacer formation is well-known in the art. Spacers 408 are typically made of silicon nitride. However, it should be appreciated by those of ordinary skill in the art that spacers 408 may be made from other dielectric materials and may include a single dielectric layer, such as silicon dioxide, or several layers formed by various methods. In one embodiment, each spacer

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408 is comprised of oxide layer 410 of silicon dioxide. An adhesion layer 412 of silicon oxynitride is formed when the silicon dioxide layer is exposed to a plasma treatment of nitrous oxide gas. In the embodiment described above, a passivation layer 414 made of silicon nitride, for example, is formed over adhesion layer 412, resulting in a strong chemical bond between oxide layer 410 and passivation layer 414. Gate 404 is separated from substrate 400 by intermediate layer 402.

IN THE CLAIMS

The claims are amended as follows:

17. (Amended) An integrated circuit (IC) comprising:

an ~~insulating~~ oxide layer;

an adhesion layer formed over said ~~insulating~~ oxide layer; and~~,~~

a first passivation layer formed on said adhesion layer, said first passivation layer and said adhesion layer including at least one common chemical element.

19. (Amended) The integrated circuit of claim 17 wherein said ~~insulating~~ oxide layer includes silicon dioxide (SiO_2).

23. (Amended) An integrated circuit comprising in a three layer stack:

a silicon dioxide insulating layer;

a silicon oxynitride adhesion layer formed ~~over~~ on said silicon dioxide insulating layer; and~~,~~

a silicon nitride hard passivation layer formed on said silicon oxynitride adhesion layer.

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